Project ID # elt246

Implementation of WBG devices in circuits, circuit topology, system integration as well as SiC devices

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This presentation does not contain any proprietary, confidential, or otherwise restricted information.

Overview

Timeline

- Project start: April 2019
- Project end: March 2024
- Percent Complete: 40%

Budget

- Total project funding: $ 1.5 M
- BP1 funding: $ 300 K

  BP2 funding: $ 300 K

  BP3 funding: $ 300 K

Barriers

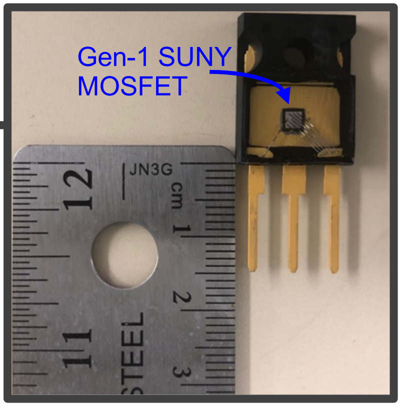
- Commercial devices are not ready for insertion into a vehicle power train for long operational life.
- A comprehensive reliability study will be undertaken for currently available commercial devices and better devices will be designed.

Partners

- Sandia National Laboratories
- SUNY POLYTECHNIC INSTITUTE,

  Albany, NY

Approach



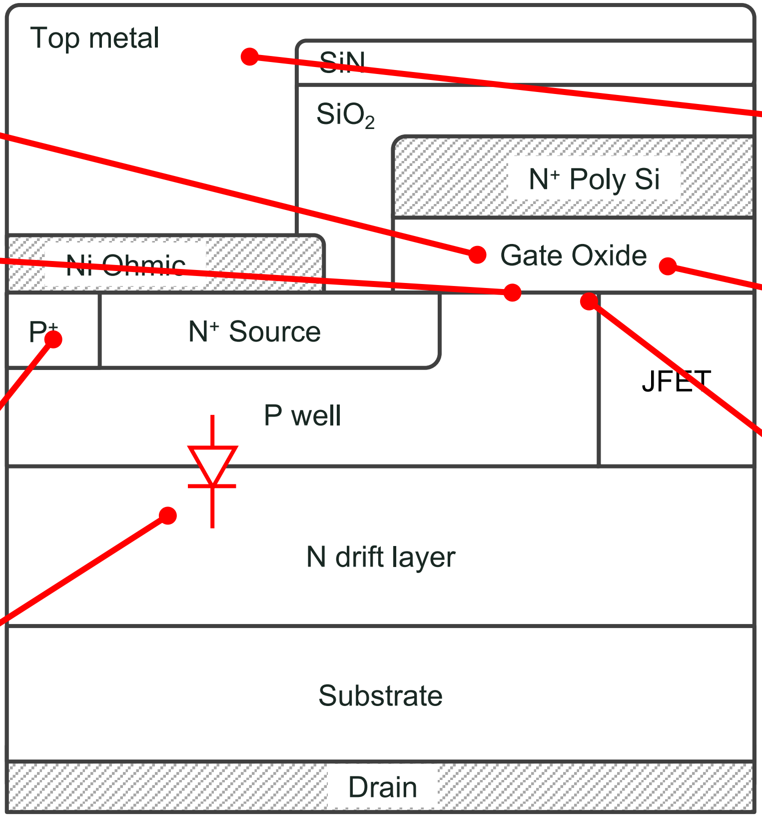
Reliability/ruggedness evaluation of SUNY MOSFETs

Threshold Voltage Instability

- **Poor Gate Oxide Reliability : Positive & Negative V_{th} Shift**
- **High Electric Field : V_{th} Shift**

Body Diode Degradation

- **Room Temp. Implanted P^+ : Cause Basal Plane Dis.**
- **Basal Plane Dis. in Epi : Expansion to Stacking Fault**



Short Circuit Withstand Time

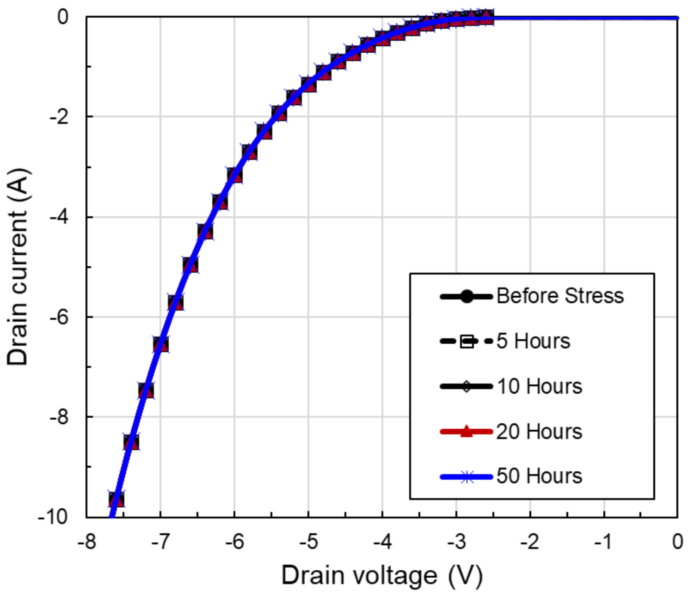
- **Al Overlayer (melting at 660°C): Metal Melting & Reconstruction**
- **Thin Gate Oxide : Higher Gate Leakage Current**
- **Short Channel : 2-3μs Short Circuit Time**

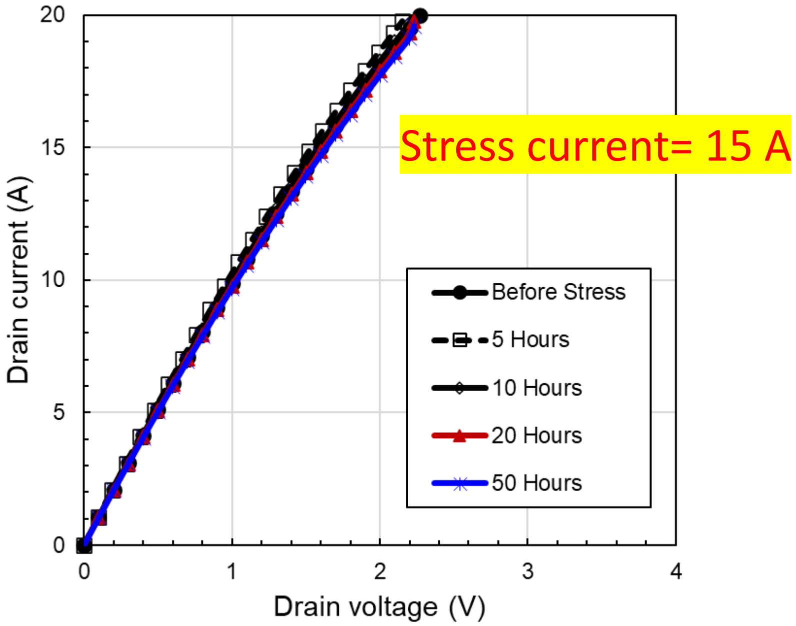
Technical Accomplishments and Progress

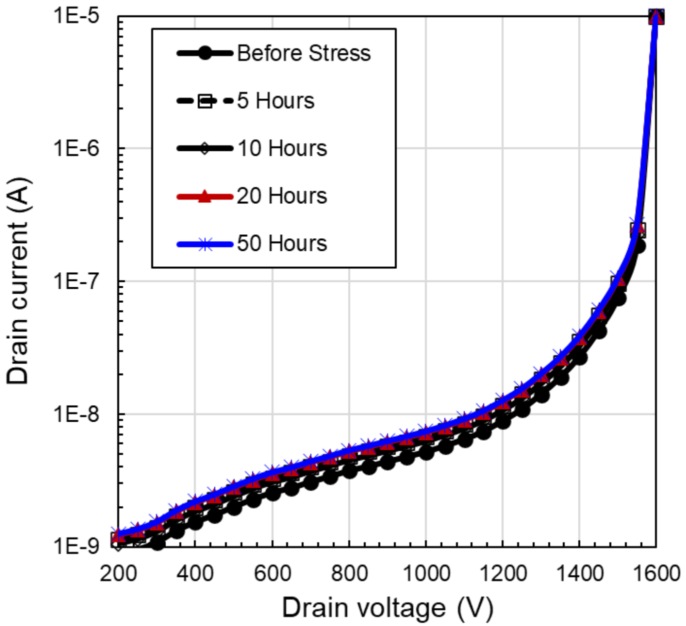
Reliability evaluation of SiC devices

B. Body Diode Degradation

- All tested Gen-1 devices with RT implants didn't show any body diode degradation





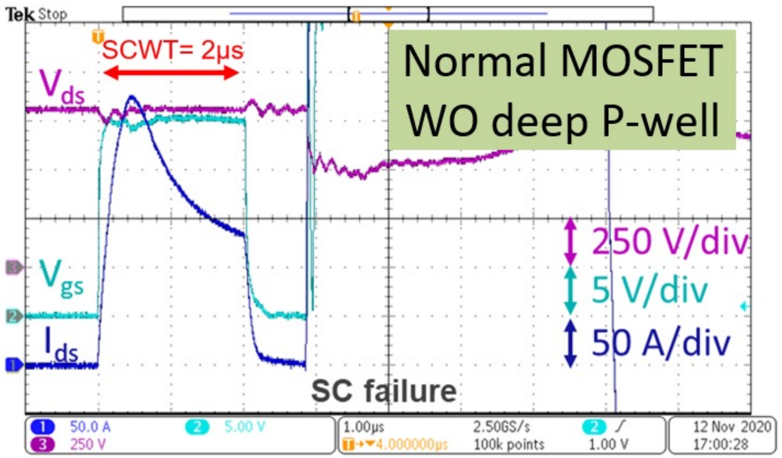


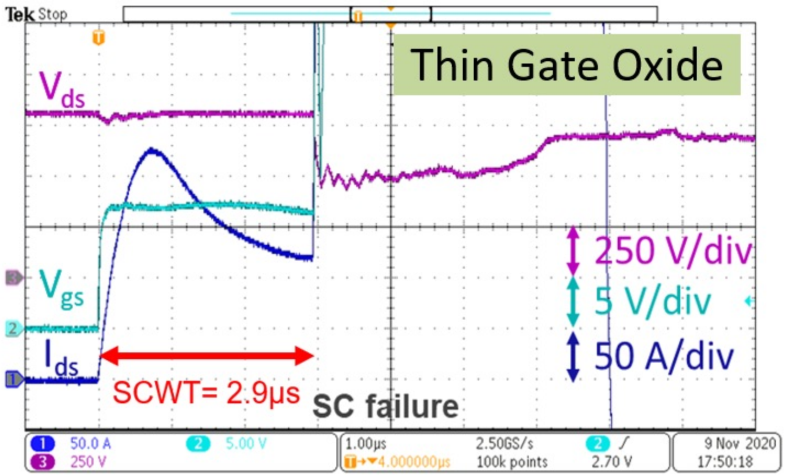
Room Temperature Implants can be used w/o body diode degradation for 1200 V MOSFETs – 30% cost savings

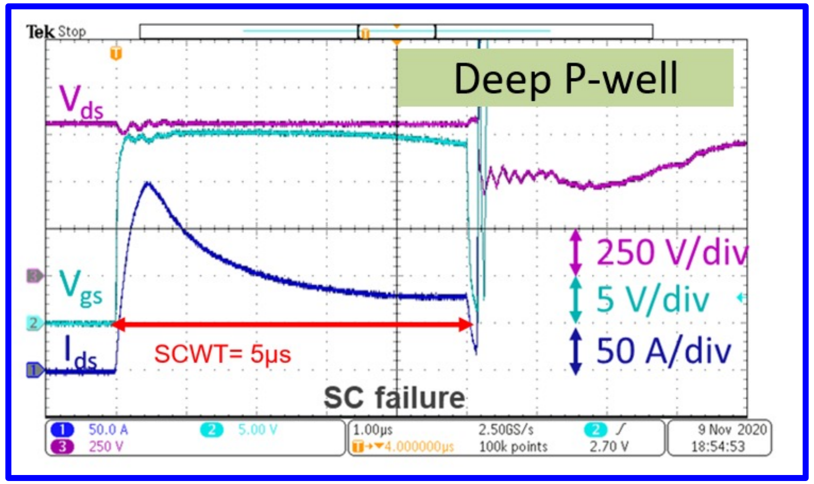
Technical Accomplishments and Progress

Reliability evaluation of SiC devices C. Short Circuit Withstand Time

Gen-1 SUNY Poly MOSFETs





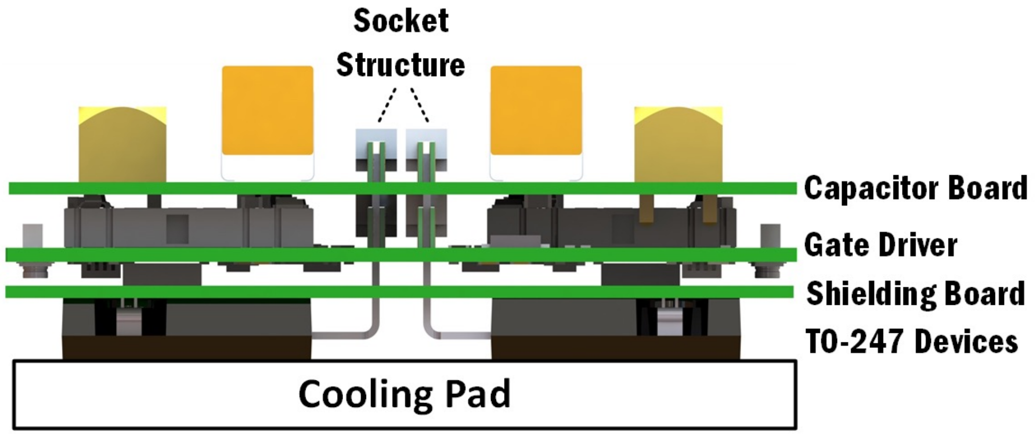


Deep p-well improves Short Circuit Withstand Time by 2.5x
This represents major technical breakthrough
10 us is possible by other design changes

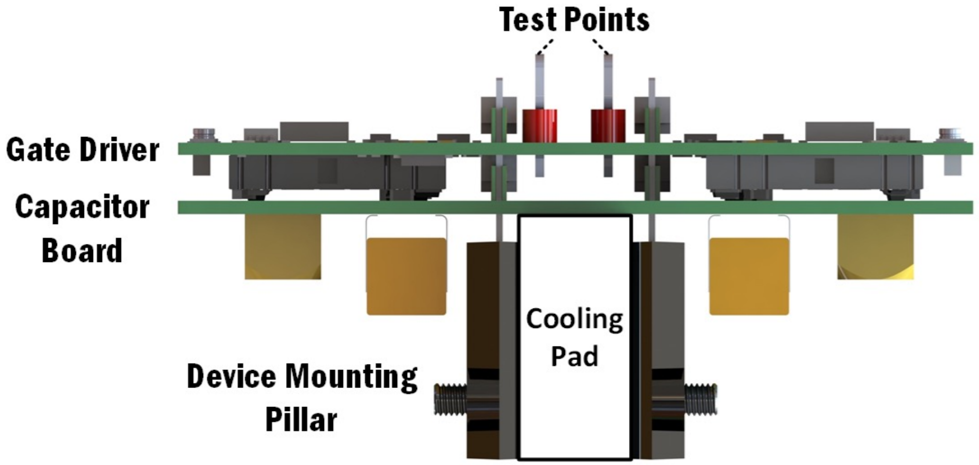
10 kVA 3-phase Inverter-II Design

The newly designed Inverter-2 improves reliability and noise immunity through few modifications:

- The new design inverter layout is simplified, since the gate driver is no longer sandwiched in between switching devices and capacitor board, the interference can be mitigated and shielding layer is eliminated
- Shorter power loop reduces stray inductance and noise coupling
- The assembly and test are easier with improved mechanical design



Inverter-1

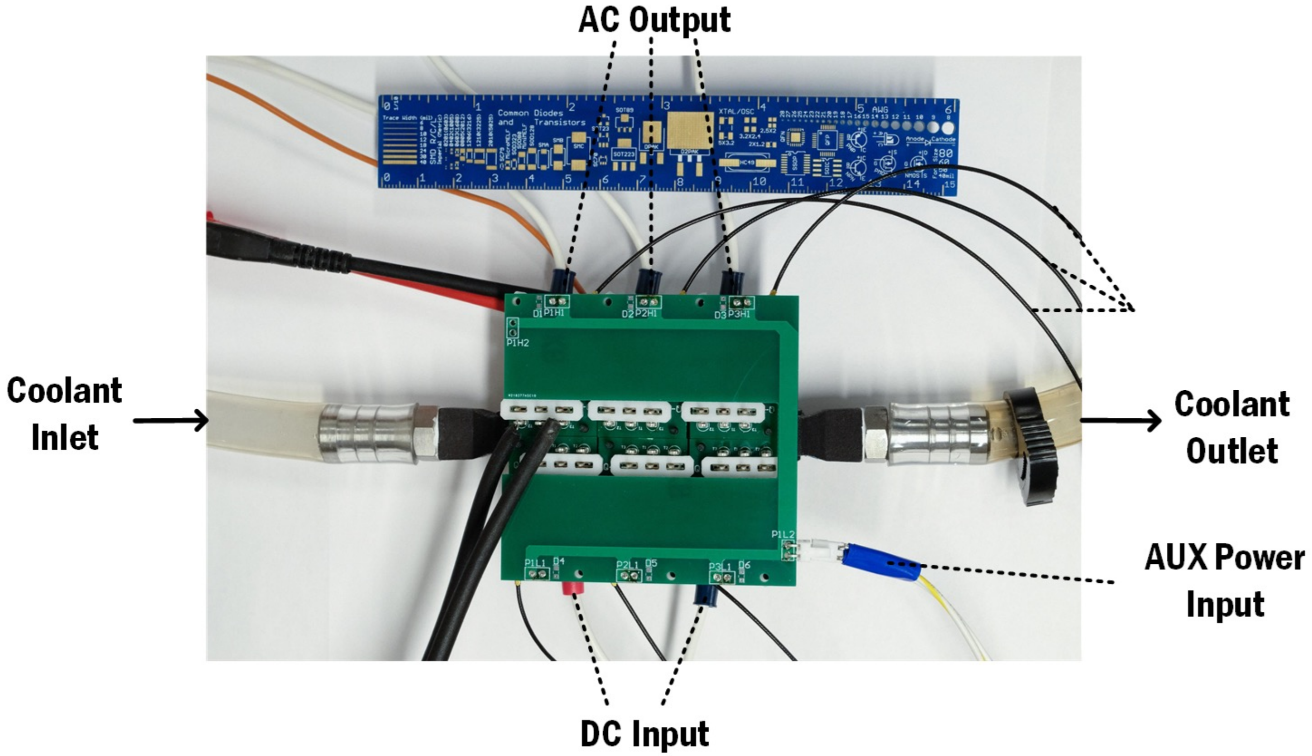


Inverter-2

10 kVA 3-phase Inverter-II Design

Inverter Test Condition

- Inverter operates under full load to stress the devices and cooling system, circuit robustness is also evaluated during the operation



Test Setup

Test Conditions

Parameters	Value
Output Power	0-11 kVA
Input Voltage	0-800 V
Switching Frequency	30 kHz
L_{Load}	100 mH
R_{load}	10 Ω
Measured Items	V_{gs} (Lower Device), V_{line}, V_{in}, I_{out}, $T_{thermal\_pad}$
Thermal Measurement	Thermal Gun/Couple

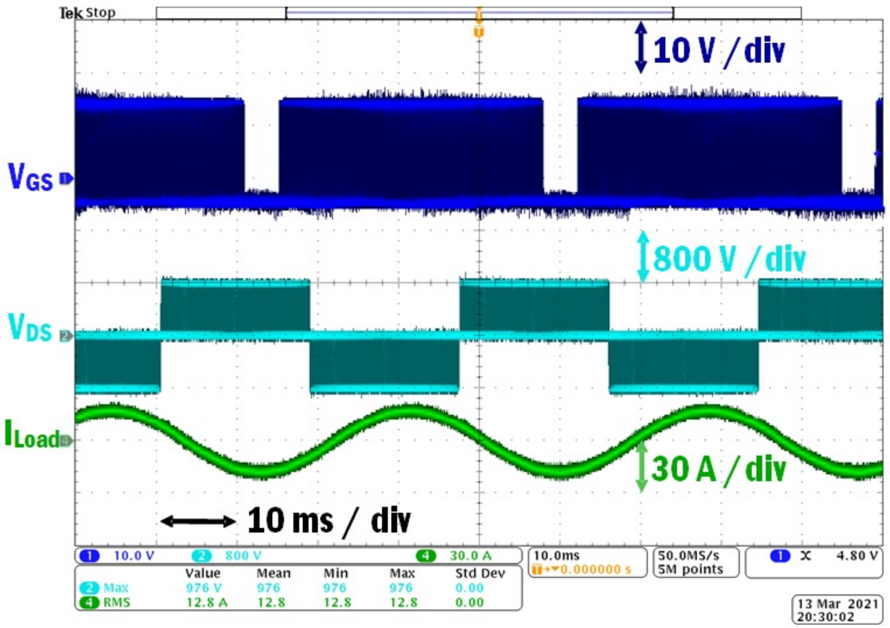
Technical Accomplishments and Progress

Prof. Jin Wang

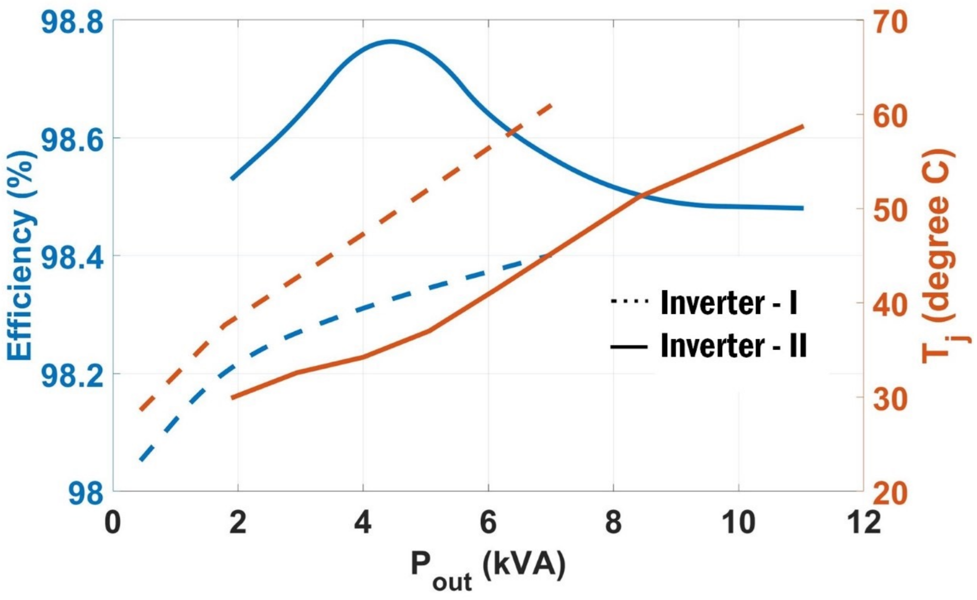
10 kVA 3-phase Inverter-II Design

Inverter Test Results

- Based on the test, inverter can reach the power density of **77 kVA/L** with reactive load
- The gate driver works well despite being in harsh EMI condition
- With effective cooling system, the maximum junction temperature of MOSFETs is lower than 60°C at 11 kVA output power



Inverter Operation Waveform



Efficiency & Estimated $T_{junction}$ with Output Power

Technical Accomplishments and Progress

Prof. Jin Wang

10 kVA 3-phase Inverter-II Design

Inverter-I and Inverter-II Comparison

Inverter I

Parameters	Value
Output Power	0-7 kVA
Input Voltage	0-800 V
Switching Frequency	30 kHz
L_{Load}	240.5 µH
R_{Load}	33 Ω
Measured Items	V_{gs} (Lower Device), V_{line}, V_{in}, I_{out}, $T_{thermal\_pad}$
Thermal Measurement	Thermal Gun/Couple
Size	70*63*32 mm = 0.145 L
Power Density	69 kVA/L

Inverter II

Parameters	Value
Output Power	**0-11 kVA**
Input Voltage	0-800 V
Switching Frequency	30 kHz
L_{Load}	**100 mH**
R_{Load}	**10 Ω**
Measured Items	V_{gs} (Lower Device), V_{line}, V_{in}, I_{out}, $T_{thermal\_pad}$
Thermal Measurement	Thermal Gun/Couple
Size	70*71*29.5 mm = **0.146 L**
Power Density	**77 kVA/L**

Proposed Future Research

Stand-alone device failure mechanism tests on Gen-2 devices:

Body diode stability, threshold voltage stability, short circuit time and avalanche energy tests will be evaluated

Gen-2 devices will be evaluated with Inverter-3:

Gen-2 devices fully will be evaluated with the Inverter-3 at accelerated temperature and power cycles

Summary

- Room Temperature Implants can be used w/o body diode degradation for 1200 V MOSFETs. 30% cost reduction.
- Short Circuit withstand time has been increased to 6 us. 10 us can be achieved in future.
- Newly designed 10 kVA three-phase inverter delivers higher power density, better reliability and efficiency.
- Inverter-2 is stressed under full load, the performance of new designed cooling system is improved.
- We will work with SUNY Poly to re-design more reliable devices